I claim:

1. An integrated memory, comprising:

address inputs for receiving a latency value and one of a row address and a column address;

an instruction decoder having a signal input and a signal applied to said signal input being used to determine whether an address applied to said address inputs being the row address or the column address; and

an evaluation unit connected downstream of said instruction decoder and having evaluation inputs connected to said address inputs and an output, said evaluation unit producing a latency signal corresponding to the latency value after receiving the column address and the latency value, the latency signal being available at said output.

2. The memory according to claim 1, wherein said instruction decoder has an instruction input for receiving an access instruction, said instruction decoder sending a control signal to said evaluation unit upon receiving the access instruction, and said evaluation unit producing the latency signal upon receiving the control signal.

3. The memory according to claim 1, wherein said evaluation inputs are connected to said address inputs carrying most significant address bits.

4. The memory according to claim 1, further comprising a further evaluation unit having further evaluation inputs and a further output, said further evaluation unit connected downstream of said instruction decoder and said further evaluation inputs are connected to said address inputs, said further evaluation unit upon receiving the column address and the latency value, in conjunction with said instruction decoder decoding a write instruction, produces a write latency signal available at said further output.

5. The memory according to claim 4, further comprising:

a data path connected downstream of said evaluation unit;

drivers, including input drivers and output drivers connected to said data path; and

a memory array connected to said data path, said data path switches data from said memory array to said output drivers on a basis of the latency signal prescribed by said evaluation unit.

6. The memory according to claim 5, wherein said data path switches further data from said input drivers to said memory array on a basis of the write latency signal prescribed by said further evaluation unit.

7. The memory according to claim 4, further comprising an address buffer connected between said address inputs and said evaluation inputs and said further evaluation inputs.

8. The memory according to claim 4, further comprising an instruction buffer connected between said instruction decoder and each of said evaluation unit and said further evaluation unit.

9. A method for setting a latency in an integrated memory, which comprises the steps of:

applying a column address and a latency value to address inputs of the integrated memory;

carrying out a check to determine if the integrated memory has a memory access instruction applied to it; and

using an evaluation unit to produce a latency signal on a basis of the latency value if the memory access instruction has been applied.

10. The method according to claim 9, which further comprises generating the memory access instruction if a read instruction or a write instruction is decoded.